

**AMENDMENTS TO THE CLAIMS**

***This listing of claims will replace all prior versions, and listings, of claims in the application:***

**Listing of Claims**

1. (Previously presented) A transistor comprising:  
a stack comprising:  
a silicon on insulator layer having a plurality of channels;  
a silicon oxide insulation layer adjacent the silicon on insulator layer; and  
a dielectric layer adjacent the silicon oxide insulation layer; and  
a gate electrode,  
wherein the gate electrode covers a portion of the stack;  
wherein at least one channel has a gate configuration that is different than remaining channels of the plurality of channels.
2. (Original) The transistor according to claim 1, wherein the at least one channel has a first thickness that is greater than the thickness of the remaining channels.
3. (Original) The transistor according to claim 1, wherein the at least one channel has a different gate dielectric than the remaining channels.
4. (Original) The transistor according to claim 3, wherein the gate dielectric of the at least one channel is a high-k dielectric, and the gate dielectric of the remaining channels is a material selected from the group comprising silicon dioxide, nitride oxide, and a silicon oxide that has undergone a plasma nitridation process.
5. (Original) The transistor according to claim 1, wherein the stack further comprises a protection layer located between the dielectric layer and the gate electrode.
6. (Original) The transistor according to claim 5, wherein the protection layer is a metal.

7. (Original) The transistor according to claim 5, wherein the protection layer is a thin polysilicon.

8. (Original) The transistor according to claim 1, wherein the dielectric layer is a high-k dielectric material.

9. (Original) The transistor according to claim 1, wherein the stack and the gate electrode are incorporated into a finFET device.

10. (Original) A transistor comprising:  
a stack comprising:  
a silicon on insulator layer;  
a silicon oxide insulation layer on the silicon on insulator layer;  
a dielectric layer on the silicon oxide insulation layer, wherein the dielectric layer is a high-k dielectric material; and  
a protection layer on the dielectric layer; and  
a gate electrode covering a portion of the stack.

11. (Original) The transistor according to claim 10, wherein the protection layer is a metal.

12. (Original) The transistor according to claim 10, wherein the protection layer is a polysilicon.

13. (Original) The transistor according to claim 10, wherein the stack and the gate electrode are incorporated into a finFET device.

Claims 14. – 20. (Canceled).

21. (New) The transistor according to claim 1, wherein the stack is arranged such that the silicon on insulator layer, the silicon oxide insulation layer, and the dielectric layer are located one on top of the other.

22. (New) The transistor according to claim 10, wherein the stack is arranged such that the silicon on insulator layer, the silicon oxide insulation layer, and the dielectric layer are located one on top of the other.